**CLAIMS:**

What is claimed is:

1. A method of reducing power consumption of a clocked circuit containing a plurality of latches, the method comprising the steps of:

locating, within the plurality of latches, a first latch in the clocked circuit having more than a predetermined slack period;

determining availability of a second latch having more than a zero slack period; and

replacing the first latch with the available second latch.

2. The method as recited in claim 1, wherein the clocked circuit also contains a plurality of local clock buffers, further comprising:

locating, within the clocked circuit, one or more local clock buffers within the plurality of local clock buffer, wherein a first clock buffer has a reduced clock load;

determining the availability of a second local clock buffer, wherein the second local clock buffer drives a lower power load; and

replacing the first local clock buffer with the available second local clock buffer.

3. The method as recited in claim 2, wherein the first local clock buffer is a high clock power local clock buffer.

4. The method as recited in claim 2, wherein the second local clock buffer is a low clock power local clock buffer.

5. The method as recited in claim 1, wherein replacing the first latch with the second latch forms a modified clocked circuit and further comprising:

testing the modified clock circuit; and

responsive to the modified clock circuit failing the test, inserting the first latch back into the clocked circuit.

6. The method as recited in claim 5, wherein a timing test tests the modified clock circuit.

7. The method as recited in claim 1, wherein the first latch is a high power consumption latch.

8. The method as recited in claim 1, wherein the plurality of latches is a plurality of high power consumption latches.

9. The method as recited in claim 1, wherein the second latch is a low power consumption latch.

10. The method of claim 1, wherein the predetermined slack period is at least one of an input slack period and an output slack period.

11. The method as recited in claim 10, wherein the input slack period is greater than 100 picoseconds.

12. The method as recited in claim 10, wherein the output slack period is greater than 300 picoseconds.

13. An apparatus for reducing power consumption of a clocked circuit containing a plurality of latches, comprising:

a first latch;

a timing device; and

a second latch, wherein the first latch is located in the clocked circuit having more than a predetermined slack period by the timing device, availability of the second latch having more than a zero slack period is determined by the timing device, and the first latch is replaced with the available second latch.

14. The apparatus as recited in claim 13, wherein the first latch is a high power consumption latch.

15. The apparatus as recited in claim 13, wherein the second latch is a low power consumption latch.

16. An apparatus for reducing power consumption of a clocked circuit containing a plurality of latches, comprising:

locating means for locating, within the plurality of latches, a first latch in the clocked circuit having more than a predetermined slack period;

determining means for determining availability of a second latch having more than zero slack period; and

replacing means for replacing the first latch with the available second latch.

17. The apparatus as recited in claim 16, wherein the clocked circuit also contains a plurality of local clock buffers, further comprising:

locating means for locating, within the clocked circuit, one or more local clock buffers within the plurality of local clock buffer, wherein a first local clock buffer has a reduced clock load;

determining means for determining the availability of a second local clock buffer, wherein the second local clock buffer drives a lower power load; and

replacing means for replacing the first local clock buffer with the available second local clock buffer.

18. The apparatus as recited in claim 17, wherein the first local clock buffer is a high clock power local clock buffer.

19. The apparatus as recited in claim 17, wherein the second local clock buffer is a low clock power local clock buffer.

20. The apparatus as recited in claim 16, wherein replacing the first latch with the second latch forms a modified clocked circuit and further comprising:

testing means for testing the modified clock circuit; and

inserting means, responsive to the modified clock circuit failing the test, for inserting the first latch back into the clocked circuit.

21. The apparatus as recited in claim 20, wherein a timing test tests the modified clock circuit.

22. The apparatus as recited in claim 16, wherein the first latch is a high power consumption latch.

23. The apparatus as recited in claim 16, wherein the plurality of latches is a plurality of high power consumption latches.

24. The apparatus as recited in claim 16, wherein the second latch is a low power consumption latch.

25. The apparatus as recited in claim 16, wherein the predetermined slack period is at least one of an input slack period and an output slack period.

26. The apparatus as recited in claim 25, wherein the input slack period is greater than 100 picoseconds.

27. The apparatus as recited in claim 25, wherein the output slack period is greater than 300 picoseconds.